an isolation structure located in the trench;

Cont'd A1

a sidewall spacer located over at least one sidewall of the trench distal the channel region;

and

a source/drain region located over the isolation structure.

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(2) Kindly rewrite Claim 5 as follows:

5. (Amended) The semiconductor device as recited in Claim 1 wherein an oxide layer is located between the sidewall spacer and the at least one sidewall of the trench.

A2

(3) Kindly rewrite Claim 6 as follows:

6. (Amended) The semiconductor device as recited in Claim 1 wherein the sidewall spacer comprises a nitrided layer.

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(4) Kindly rewrite Claim 9 as follows:

9. (Amended) A method of manufacturing a semiconductor device, comprising:

A3

forming a channel region in a semiconductor substrate;

forming a trench adjacent a side of the channel region;

forming an isolation structure in the trench;

forming a sidewall spacer over at least one sidewall of the trench distal the channel region;

and

forming a source/drain region over the isolation structure.

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(5) Kindly rewrite Claim 13 as follows:

13. (Amended) The method as recited in Claim 9 further including forming an oxide layer between the sidewall spacer and the at least one sidewall of the trench.

A4

(6) Kindly rewrite Claim 14 as follows:

14. (Amended) The method as recited in Claim wherein forming a sidewall spacer includes forming a nitrided layer.

(7) Kindly rewrite Claim 17 as follows:

17. (Amended) An integrated circuit, comprising:

semiconductor devices, including;

a channel region located in a semiconductor substrate;

A5

a trench located adjacent a side of the channel region;

an isolation structure located in the trench;

a sidewall spacer located over at least one sidewall of the trench distal the channel region; and

a source/drain region located over the isolation structure; and

dielectric layers located over the semiconductor devices and having interconnect structures located therein that electrically connect the semiconductor devices to form an operative-integrated circuit.

(8) Kindly add Claim 21 as follows:

A6

--21. (New Claim) The semiconductor device as recited in Claim 1 wherein the sidewall spacer is not contiguous the side of the channel region.--